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Silicon Bipolar Microwave Power Transistors

RICHARD ALLISON

Invited Paper

***Abstract*—This paper presents a review of the present status of commercially available silicon bipolar transistors and projects what power at frequency performance will be available in the next few years. It discusses the need for implementing certain fabrication/processing developments necessary to meet the projected power at frequency performance levels.**

I. Introduction

THIS ARTICLE is in the form of a review discussing the present status of commercially available silicon bipolar transistors relative to GaAs FET R&D developments. The article also projects what power at frequency performance will be available in the next few years. It discusses the need for implementing certain fabrication/processing developments necessary to meet the projected power at frequency performance levels.

It is interesting to contemplate the data summarized in Fig. 1. First, it is clear that the data fit a $Pf^2 = \text{constant}$ equation (where P = power-out, and f = frequency). Second, both GaAs FET's and Si bipolar transistors' pulse data fit a single line. The implication is that, from a peak power capability standpoint, there is little difference in performance between silicon bipolar and GaAs FET's at the present state of their development, probably because the present FET structures are not optimized to take advantage of the inherently superior GaAs properties. Third, the CW capabilities of silicon bipolars are lower than their pulse power levels by a factor of about 1.8, because the operating junction temperature is lower for pulsed operation than for CW at fixed power and efficiency. This is due to the reduced thermal interference between adjacent transistor cells whenever the pulse period is less than the transistor thermal time constant. Effectively, Θ_{jc} is improved under pulsed conditions, allowing higher power to be attained. The comparison here cannot be exact between GaAs FET's and silicon bipolars because they are not in a common package configuration. However, there is definitely the need for the thermal resistance Θ_{jc} of Si bipolars to be reduced in order to raise their CW power capabilities to the levels achieved under pulse conditions.

Since one can sacrifice gain in order to gain power, the discussion of Fig. 1 would not be complete without reference to Table I where the data used in the Pf^2 plot are shown indicating the gains and the power added efficiencies associated with those power levels. Unlike silicon bipolar devices, the GaAs FET's can be driven to higher power by allowing gain compression, and the data in Table I are in effect power-out levels achieved under drive conditions such as to maintain gains to about 4-dB levels.

In comparison to silicon bipolar transistors, the higher scatter-limited velocity and the absence of minority carriers in GaAs FET's have made GaAs FET's applicable for high-frequency operation. However, developments in bipolar technology are in progress that will substantially increase the frequency capability by increasing both

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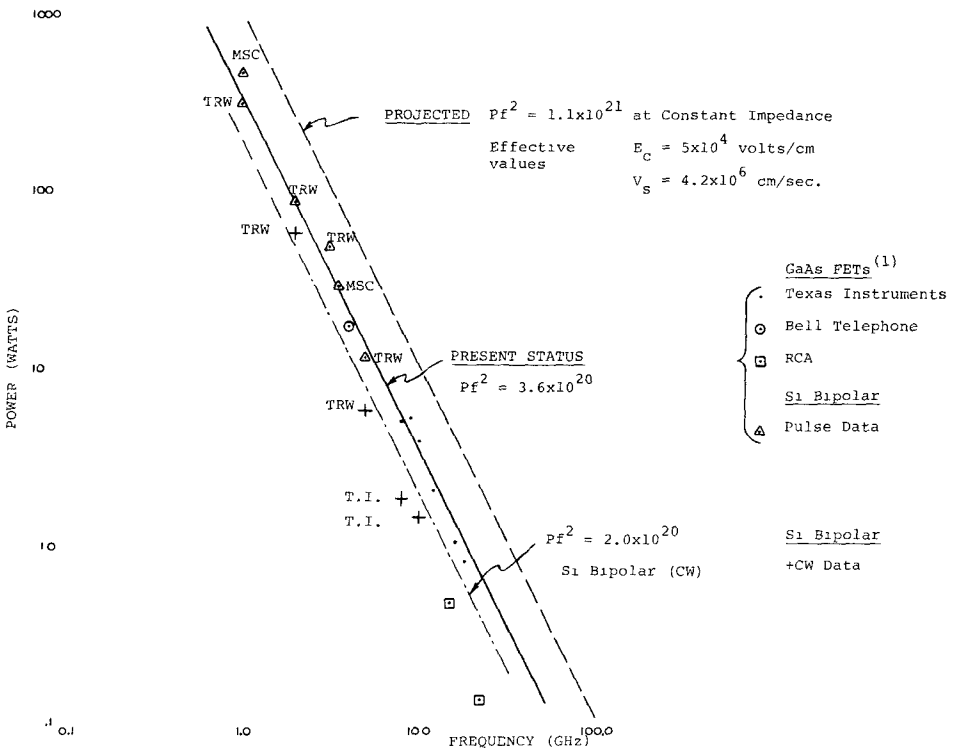

Fig. 1. State-of-the-art performance of microwave power transistors.

TABLE I

Frequency (GHz)	P_o (watts)	Associated Gain (dB)	ηPA (%)	Source
GaAs FET				
4	18	- -	- -	Bell Labs
8	5.13	5	34.6	T.I.
9	5.31	4.2	19.2	T.I.
10	4.17	4.3	24.9	T.I.
12	2.10	4.0	17.0	T.I.
15	0.50	3.0	25.0	RCA
16	1.10	4.0	30.4	T.I.
18	0.85	4.0	23.8	RCA
22	0.14	4.8	9.0	RCA
Silicon Bipolar				
1	480 (Pulse)	- -	- -	MSC
1	320 (Pulse)	7	39.2	TRW
2	90 (Pulse)	9	43.1	TRW
2	60 (CW)	11	46.3	TRW
3.1	50 (Pulse)	7.1	36.4	TRW
3.5	30 (Pulse)	- -	- -	MSC
5.0	12 (Pulse)	7.2	24.4	TRW
5.0	6 (CW)	7.0	25.2	TRW
8.0	1.9 (CW)	5.6	25.6	T.I.
10.0	1.5 (CW)	3.5	14.0	T.I.

f_T and reducing collector-base time constants, two necessary conditions for high-frequency operation as discussed below.

The general form for the gain of a transistor as a function of frequency is

$$G(f) \approx \frac{G_0}{\left[1+G_0^2\left(\frac{f}{f_{\max}}\right)^4\right]^{1/2}}$$

when

$$G_0^2\left(\frac{f}{f_{\max}}\right)^4 \gg 1$$

then

$$G = Z\left(\frac{f_{\max}}{f}\right)^2$$

and gain falls off at 6 dB per octave where $f_{\max}$ is the maximum frequency of oscillation and is defined as the frequency at which the transistor unilateral power gain equals unity. The proportionality constant Z, which accounts for the transistor parasitic elements, typically ranges from 0.2 to 0.3. Therefore, for a transistor to be able to generate useful power gain, for example, at 10 GHz, the $f_{\max}$ of the transistor must be approximately 25 GHz.

Pritchard [2] derived a figure of merit K (assuming $\alpha_0 = 1$):

$$K = (\text{power gain})^{1/2} \qquad \text{bandwidth} = \left(\frac{f_T}{8\pi r_b' C_c}\right)^{1/2}$$

where

f_T transistor current gain–bandwidth product,
$r_b' C_c$ collector-base time constant.

At a power gain equal to 1, the maximum frequency of oscillation $f_{\max}$ can be defined as

$$f_{\max} = \left(\frac{\alpha_0 f_T}{8\pi r_b' C_c}\right)^{1/2}$$

where α_0 is the common-base dc gain.

The emitter and base pattern may be defined, in a simple way, in terms of the emitter stripe width S and emitter stripe length l. Let R_{BB} represent the sheet resistance of the base, and C_0 the capacitance per unit area. Then

$$r_b' \propto R_{BB}\frac{S}{l} \text{ and } C_c \propto C_0 Sl$$

then

$$f_{\max} \propto \frac{1}{S}\left[\frac{\alpha_0 f_T}{8\pi R_{BB} C_0}\right]^{1/2}.$$

For a transistor operating at X band, f_T needs to be approximately 10 GHz, and this can be accomplished by shallow arsenic emitter processes. To get $f_{\max}$ to the required 25-GHz levels, it is necessary to get the $r_b' C_c$ time constant down to 0.7 ps. It is seen from the above equation that the best approach to achieve this reduction is by reducing the emitter stripe width S, X band, and higher frequencies requiring micrometer and submicrometer stripe widths.

To be able to achieve this level of linewidth definition, the development of lithographic processes dependent on deep UV, X-ray, e-beam, etc., is required. In addition, these linewidths, once exposed, must be defined by etching processes which reproduce the mask faithfully. Plasma etching, ion milling, etc., are processes under development. Both subjects will be discussed below.

II. Vertical Technology

Maximization of $f_{\max}$, aside from lithographic issues, are dependent on maximizing f_T, and minimizing the $r_b C_c$ product.

A. $f_{\max}$

Transistor frequency response is limited by charge carrier delay in the emitter, base, and collector regions. It is important to understand how physical parameters govern carrier transit times throughout the vertical structure in order to optimize high-frequency performance. The recent use of arsenic instead of phosphorus emitters, and of the ion implantation of emitter and base junctions, has produced microwave transistors which exceed previous frequency limitations by 50 percent.

Total signal delay time from emitter to collector (n-p-n transistor)

$$\frac{1}{2\pi f_T} = \tau_{ec} = \frac{X_{jeb}^2}{2D_{pe}\beta_0} + r_e(C_{eb} + C_n + C_{tc}) + \frac{W_b^2}{nD_{nb}} + \frac{W_b}{V_s} + \frac{X_d}{2V_s} + r_c C_{tc}$$

where

- f_T frequency where current gain becomes unity,
- τ_{ec} total carrier transit time from emitter to collector,
- X_{jeb} depth of emitter junction,
- D_{pe} diffusivity of holes in the emitter,
- β_0 dc gain,
- r_e emitter resistance,
- C_{eb} emitter base diffusion capacitance,
- C_n emitter neutral capacitance,
- C_{tc} collector capacitance,
- W_b basewidth from emitter to collector,
- n factor for electric field in the base,
- D_{nb} diffusivity of electrons in the base,
- V_s scatter limited velocity of silicon,
- X_d collector space charge width,
- r_c collector resistance.

This is different than the usually seen equation by four factors, which will now be discussed.

1) DeMan [3] showed that heavy emitter doping caused an additional delay of

$$\tau_e = \frac{Q_e}{I_c} = \frac{1}{\beta_0}\int_0^{\dot{X}_{eb}} \frac{n_{ie}^2}{N}\left(\int_0^x \frac{N}{D_{pe}n_{ie}^2}\,dx\right)dx$$

where

- Q_e excess charge in emitter,
- $\dot{X}_{eb}$ boundary between emitter neutral region and the E–B space-charge region.

This expression accounts for impurity level broadening and band-edge tails caused by high doping of the emitter, which is concomitant with a reduction of the Si band gap.

For arsenic, n_{ie} is smaller than for phosphorus because of the better ionic fit. In addition, the arsenic profile is relatively flat-topped, allowing us to reduce the above equation to [4]

$$\tau_e = \frac{X_{jeb}^2}{2D_{pe}\beta_0}.$$

To reduce this delay we must make the emitter as shallow as possible and the emitter concentration as low as possible for D_{pe} to have a high value. In addition, we must make β_0 as high as possible, which can be done by increasing the emitter concentration (a compromise has to be made here due to the above discussion of band-gap narrowing), or narrowing the basewidth.

Including this term in this transit time calculation reduces the f_T by 50 percent as shown by DeMan [3], and brings the theoretical calculations closer to the experimentally measured f_T's.

2) Kirk [5] has pointed out that, due to the nonzero value of the charge density in the base (usually it is assumed that the concentration gradient in the base goes to zero at the collector junction, requiring an infinite mobility to account for a finite collector current), an additional delay comes into play equal to

$$\tau_b = \frac{W_b}{v_s}.$$

3) Emitter neutral capacitance effects, as opposed to space-charge effects, have been shown to account for 70 percent of the delay time in the emitter [6]. The additional

delay due to C_n is

$$\tau_{en} = \frac{2q\bar{N}_a W_b V}{kTaD_n}$$

where

a emitter concentration gradient,
$\bar{N}_a W_b$ average charge in base,
D_n diffusion coefficient for electrons.

This delay is dependent on the total charge in the base ($\bar{N}_a W_b$), and its reduction requires a reduction in base width or in base concentration (consistent with other device design considerations), an increase in the gradient of concentration distribution, and an increase in the diffusion coefficient of electrons which is concentration dependent. This greater D_n requires lower concentration bases.

4) The fourth point is the base transit time described by

$$\tau_b = \frac{W_b^2}{nD_{nb}}.$$

The factor n, accounting for the effect of the electric field due to the ionized impurities, can have values between 4 to 7, depending on the diffusion profile (Gaussian, exponential, etc.). This higher n value is mitigated by the lower D_{nb} values for higher concentration near the emitter. In addition, at high currents this field, due to ionized impurities, it is essentially swamped by the high-mobile charges. Overall, a good approximation to n is 3–4, taking all of the above into consideration.

Basewidths less than 0.15 μm have been difficult to achieve with good yield using thermally diffused base and emitter junctions. Ion implantation offers a method of achieving <0.1-μm basewidths with excellent uniformity.

Although ion implantation has been established as an effective process for MOS devices for some time, it is only recently that ion implantation has been adapted for use in bipolar microwave devices. The higher impurity concentrations and, subsequently, the greater fluences utilized for bipolar devices result in the introduction of a level of lattice damage which requires special consideration. For fluences of the order of 5×10^{13} cm^{-2} and higher, sequential thermal oxidation results in the generation of stacking faults and the development of significant leakage [7]. The use of CVD layers for masking permits us to avoid these deleterious effects for base implantation. The higher fluences required for emitter generation result in such heavy lattice damage that the surface is converted to an amorphous state. Two techniques have been developed to successfully use emitter implantation. One is the use of a two-stage annealing treatment [8] which permits the regrowth of the amorphous layer with a significant reduction of lattice damage. The other is the use of a short drive which moves the emitter–base junction into an unimplanted and, therefore, undamaged area [9]. Within the past year, significant strides have been made in the development of laser-annealing techniques for ion-implanted surfaces. It appears possible that laser annealing will permit us to generate structures of high crystalline perfection and still maintain the precise control of the donor and acceptor profiles characteristic of ion implantation.

B. Output Power

To deliver substantial amount of power, the transistor's collector resistance needs to be as low as possible:

$$P_{\text{out}} \propto \frac{1}{R_c} = \frac{\text{area}}{\rho_c t}$$

where

t epitaxial collector thickness,
ρ_c collector resistivity,
R_c collector resistance.

The collector resistivity and thickness are usually governed by the voltage at which the transistor is designed to operate. The voltage achievable in the transistor is limited by the curvature of the base cylindrical junction which effectively limits the attainable voltage to about 30 percent of the bulk capability of the collector. This can be circumvented by depletion rings or p^+ guard-ring diffusion deeper than the main base, so that the voltage is now limited by the deeper curvature-limited junction. This helps raise the voltage to about 50 percent of bulk.

Both of these techniques force the designer to use higher resistivity material or thicker collectors than he would otherwise have utilized. By tailoring diffusion profiles, it is now possible to raise the curvature breakdown up to 90 percent of bulk levels. This allows reductions of both the resistivity and thickness of the collector, and up to 30-percent increase in P_{out} has been produced as compared to conventional collector structures.

III. Horizontal Technology

A. Lithographic Processes

Reduction in stripe width to increase $f_{\max}$ dictates the development of improved lithographic techniques for pattern definition. Table II summarizes alternative technologies.

The minimum linewidths attainable on a production basis with present state-of-the-art masks, photoresists, and contact printing using the conventional soft UV ($\lambda\simeq3000$ Å) mask aligners is on the order of 1 μm, although approximately 0.5 μm has been attained on a laboratory scale.

Several new technologies are under extensive investigation.

1) *Deep UV* exposure systems, with λ on the order of 2250 Å, have demonstrated linewidth reduction capability on the order of 5000 Å. Implementation of deep UV systems will require development of sources of optical quality quartz mask blanks (or a viable substitute) and photoresist formulations to decrease required exposure times [10], [11].

2) *X-ray exposure* systems ($\lambda\simeq10$ Å) have been demonstrated to have linewidth capabilities on the order of 1000 Å. Development of higher intensity X-ray sources, suit-

TABLE II

	λ	MIN. LINE-WIDTH RANGE	COMMENTS	TIME FRAME
Soft U.V.	2000-4000Å	1-2μ	∿1 micron linewidth	
Deep U.V.	2000-2600Å	.5-1μ	Requires quartz mask	Less than 1 year
X-ray	∿10Å	1000Å	Requires high intensity sources to reduce exposure time (e.g., Synchrotron Radiation)	2-3 years
E-Beam		400Å	High cost - likely to be used by mask makers only. Hardware, software resist techniques improvement continue over next few years.	3-5 years

able masks, and photoresists are required for implementation in production applications.

3) *Electron-beam* exposure, either for writing on the mask blank or for writing on the wafer, is another technique which is receiving a great deal of attention. The ultimate linewidth capability of this technique has been estimated variously in the range of 5–400 Å. Extensive efforts are currently underway to develop more sensitive resists and more efficient writing techniques in order to reduce exposure times. Several commercial systems are now in operation in integrated-circuit manufacturing facilities.

B. Etching Processes

The minimum etchable linewidths realizable on a production basis with wet chemical techniques are on the order of 1 μm. In order to extend etch capabilities to submicrometer geometries, newer technologies must be implemented.

Plasma etching has been demonstrated to be capable of defining submicrometer geometries. The major barrier to universal application of plasma etching is that high etch-rate ratios are not yet realizable for certain material combinations in bipolar transistor fabrication.

This technology is still in its infancy, and major advances in plasma etch capabilities are certain to take place in the near future [13]–[27].

Sputter etching and ion milling have also been demonstrated to be capable of etching geometries on the order of 0.25 μm. "Redeposition," "trenching," and ion damage to charge sensitive surfaces are the major shortcomings of these processes. Much can be done in specific processes to alleviate these problems with etch rate being the usual tradeoff.

The capability for etching of linewidths on the order of 0.5–0.25 μm is expected to be a production reality within a one-to-two-year period, with the emphasis expected to be on reactive plasma processes.

C. $r_b'C_c$ Reduction

When all the geometric factors of the transistor design contained in r_bC_c are analyzed, the equation for f_{max} becomes [28]

$$f_{max}=\left(\frac{f_T}{8\pi r_b[(k_2EP)/\delta+(k_1k_2EP)/\epsilon]}\right)^{1/2}.$$

When the geometric factors in f_T are also included, then f_{max} becomes

$$f_{max}=\left(8\pi r_bEP\left[\frac{k_2}{\gamma}+\frac{k_1k_2}{\epsilon}\right]\cdot\left\{r_e\left[\frac{k_0EP}{\delta}+\frac{k_2EP}{\gamma}+\frac{k_1k_2EP}{\epsilon}\right]+k_4\delta\left[\frac{k_2}{\delta}+\frac{k_1k_2}{\epsilon}\right]+k_3\right\}\right)^{-1/2}$$

where

EP	emitter periphery,
k_1,k_2,k_3,k_4	constants dependent on vertical geometry,
γ	EP/A_b (emitter periphery/base area),
δ	EP/A_e (emitter periphery/emitter area),
ϵ	EP/A_{pad} (emitter periphery/bonding pad area).

It is clear that maximization of f_{max} requires maximization of all three, γ, δ, and ϵ parameters. Maximization of both γ and δ factors require submicrometer photolithographic processes as discussed above. What this derivation highlights is the contribution of ϵ, which is related by dielectric thickness (SiO_2 or Si_3N_4) to C_{MOS} capacitance. It has been established that in some devices 50–75 percent of the total capacitance is made up of the MOS capacitances under the bonding pads. Optimization of the EP/C_{MOS} ratio is indicated.

Developments are in progress to deposit oxide up to 3–5-μm levels to reduce C_{MOS} capacitance, using improved CVD deposition equipment, plasma-deposition systems, and anodized porous SiO_2 deposition methods.

A second method of reducing $r_b'C_c$ without resorting to submicrometer photolithographic procedure is the development of stepped electrode transistor (SET) devices (Fig. 2), which are realized by the differential etch rate of a composite doped/undoped polysilicon emitters. Using

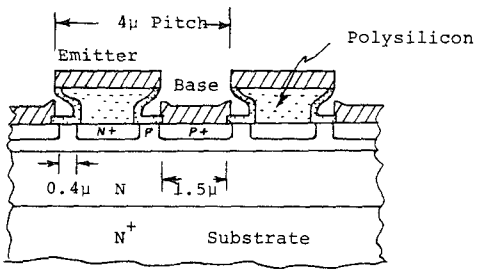

Fig. 2. Cross section of a set (stepped electrode transistor) device.

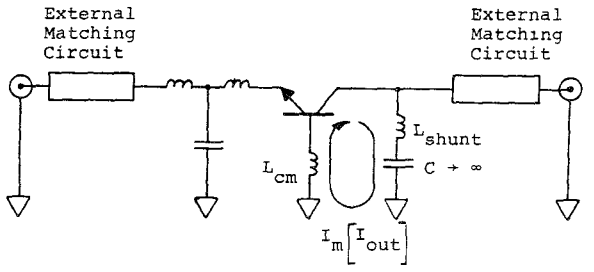

Fig. 3. Conventional shunt inductor.

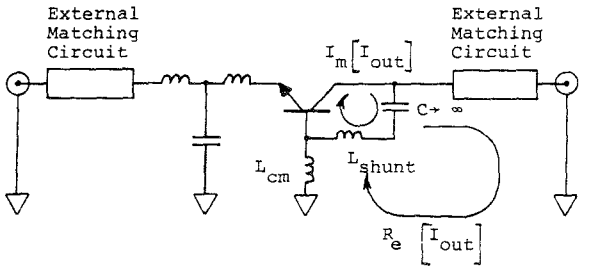

Fig. 4. Improved shunt inductor.

optical photolithograph, emitter stripe widths of submicrometer dimension can be achieved having zero-gap metal electrode spaces. Effectively, the emitter and base are separated by as little as 0.4 μm [29].

IV. Circuit Requirements and Cell Combining

Many high-power microwave applications require a transistor or amplifier to generate more power than can be supplied by a single transistor cell alone. The two common methods of combining the outputs of several devices or cells are hybrid or parallel combining. The hybrid-combining approach collects the outputs of several packaged devices in external networks and supplies the total output minus the losses of the external networks to a single output port. This technique is convenient; however, it is costly and inefficient if the number of individual devices is large.

The second approach [30], [31] is to parallel several cells in one package without the use of special combining networks. Direct paralleling of a large (>4 or 5) numbers of cells requires stringent controls on the uniformity of the individual cells, as no isolation between cells is provided by this approach. Also, identical internal-matching circuits must be used for each cell or group of cells to insure that the cells are all driven and loaded very closely in-phase. With appropriate internal circuits, many cells can be paralleled with very slight losses of performance; however, when the device becomes electrically wide, limitations arise in maintaining an equal phase condition. Also, if the device becomes very wide ($>\lambda/4$), spurious non-TEM modes may be excited in the "microstrip" package, resulting in an interesting display of instabilities.

This "maximum width" limitation will produce a point of diminishing returns in the number of cells which may be combined. Extrapolation to 10 GHz indicates a maximum of 10 or 12 cells of a nominal width of 12 mils could be combined, provided some other limit is not reached first.

The internal-matching circuitry is necessary to successfully parallel combine large numbers of cells. Above 2 GHz, the most ideal configuration for the circuitry is a separate independent input- and output-circuit section for each individual cell, such that there are no intercell transverse currents. Intracell transverse currents are allowed if each of the transverse current components is identical in magnitude and direction in each cell. This condition is also met for cell doublets, provided that all the doublets are identical.

The internal-matching network for each cell may incorporate a shunt inductor [32] to parallel resonate the output capacitance of the cell in the band of interest. Typical microwave power transistors have loaded output Q's of one to five so that the reactive portion of the output current is of a very significant magnitude. A shunt inductor placed directly across the output capacitance can route the reactive portion of the output current away from the common-mode element. Fig. 3 shows a generalized circuit of a device in which the shunt inductor L_{shunt} is connected between the collector and ground. The reactive portion of the output current $I_m[I_{out}]$ is forced to return through the common-mode inductance L_{cm}. Fig. 4 shows a modified form of the same circuit where the shunt inductor is connected between the collector and the base bonding pad. At or near resonance, the $I_m[I_{out}]$ is not required to flow in L_{cm}; only the $R_e[I_{out}]$ returns through L_{cm}. The reduced current in L_{cm} results in reduced series feedback and enhances the stability and overall performance of the device. This configuration is also conveniently realizable consistent with the circuit constraints discussed earlier. A photograph of a five-cell realization is shown in Fig. 5.

Alternative device interconnection schemes are being explored with ECOM support (Contract No. DAAB07-77-C-2689). The circuit realization shown in Fig. 4 is applicable to realization with a "beam-tape" interconnection pattern which is batch-fabricated and gang-bonded to a device. The tape interconnect pattern replaces all of the costly time-consuming wire bonding, allowing higher volume production at lower cost. The five-cell realization with the tape interconnect pattern is shown in Fig. 5.

A. Thermal Limitations

A major factor limiting the performance of microwave power transistors is junction temperature. For CW condi-

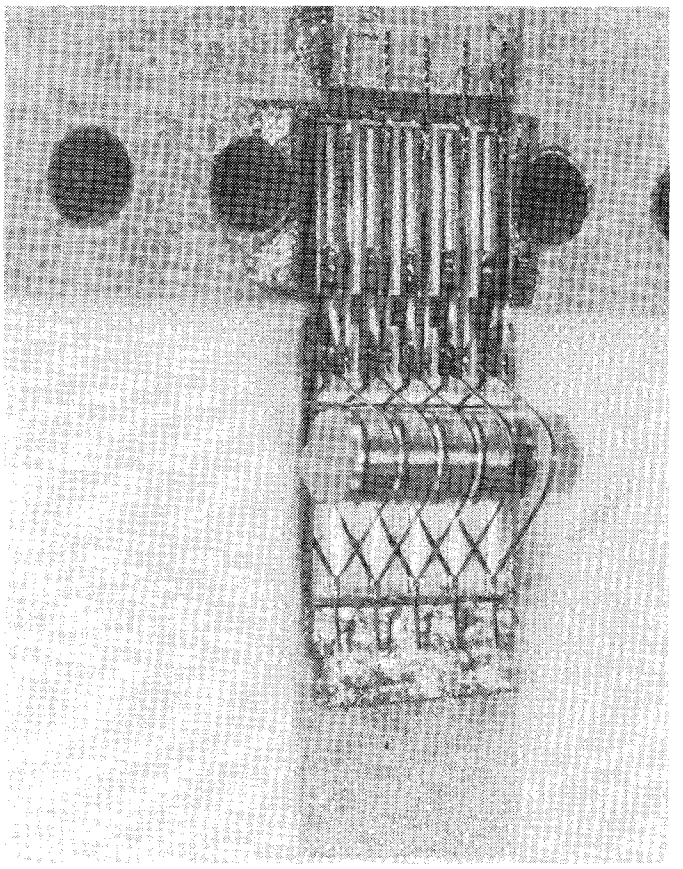

Fig. 5. Photo of 5-cell device.

tions, the cell size and shape must be carefully chosen to minimize the thermal resistance and still maintain a compact structure. State-of-the art designs have dissipated power densities of up to 5×10^4 W/cm^2 in the active area and require the beneficial effects of heat spreading in the silicon substrate to maintain the junction temperature at reasonable levels. Large edge-to-area ratios of the cell dimensions allow much of the generated heat to spread laterally. The cellular structure itself helps spread the heat generators out over larger areas of silicon and contributes to lower thermal resistance at the expense of lower packing density and fewer numbers of cells per wafer. Larger numbers of smaller cells have less thermal resistance but also have more interconnections and, therefore, higher cost.

Under short pulse conditions (<10 μs), many of the thermal issues become unimportant, and the cells can be made larger and packed tighter to improve yield and reduce cost.

B. Monolithic Integrated Circuits

The Naval Research Laboratory, under Contract No. N00173-77-C-0340, is supporting an investigation to obtain better performance at lower cost from bipolar silicon microwave transistors. The approach is to integrate the matching circuitry and active device on one chip of silicon. This will eliminate costly wire bonding and simplify the device-assembly procedure at the expense of increased chip costs. A photograph of the active device portion is shown in Fig. 6.

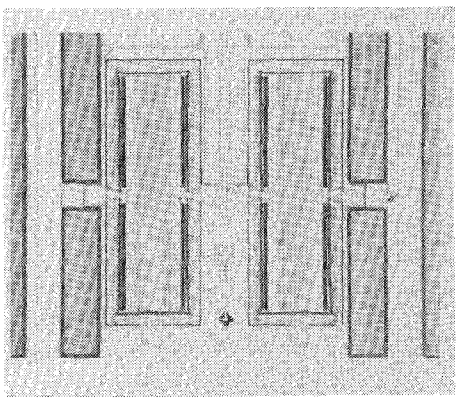

Fig. 6. Monolithic active device.

The active device is isolated from the silicon substrate by an epitaxial p-i-n structure and isolated in a horizontal direction by a polysilicon-filled V groove. The collector is brought to the top of the chip by a shallow metallized groove. This isolation and contacting scheme provides very low isolation capacitance and contact resistance. The common-mode connection is brought to the bottom of the chip by a deep metallized V groove or via. The via provides a very low inductance to ground. The chip itself can be mounted directly on a metal heat sink. The electrical isolation is provided by the p-i-n structure so that the typical BeO insulator is not necessary. Elimination of the BeO provides reduced thermal resistance and, therefore, lower junction temperatures. The reduced common-mode inductance enhances the stability of the device, and the integral-matching networks transform the device impedances to relatively high levels, allowing more convenient cell combining.

V. Reliability

The inherent reliability of bipolar transistors has been demonstrated through long-term life testing. A recently completed RF life test has shown that bipolar transistors can be operated at normal power densities and expected dissipation powers at junction temperatures of 250°C for periods in excess of 8000 h. Changes in efficiency, gain, and output power were not detected with normal measuring equipment. Delta measurements are currently in process, and a physical examination for wearout phenomena will follow.

Bipolar manufacturing technology has evolved to the point that reliable transistors are commonplace. Good die mounts are proven in a high percentage of transistors by burn-in screening. The monometallic gold on gold wire bond system employed by certain microwave houses has eliminated the formation of intermetallics that can cause eventual bond failure. This system provides reliable long pulse operation where transistor bond wires are thermomechanically flexed during long equipment lifetimes.

VI. Conclusion

It is expected that many of the techniques discussed above will be incorporated into device design and fabrication within the next two to three years and will take not only silicon bipolars, but III–V FET's as well, to higher power-frequency performance levels. What can be projected? Referring to Fig. 1 again, we have drawn a projected Pf^2 plot, which represents a threefold increase over presently realized performance. Following Johnson's [33] analysis, we believe that this projection will be realized when technological developments allow us to operate the transistor at higher "effective critical field" levels and achieve a higher "effective scattering limited velocity." In present structures, only for a small fraction of the distance that the carrier is traveling is it at scattering limited velocity, and for only a small fraction of the collector region is the field high enough to approach critical field.

The Pf^2 projection is based on the assumption that we will, in fact, have an "effective critical field" within only about 25 percent of the collector region and that the "effective scattering limited velocity" will have a value of approximately $0.7V_s = 4.2 \times 10^6$. (This 0.7 factor, implying that carriers are traveling at scattering limited velocity outside of the region in which the critical field exists, is based on the fact that the SLV is reached at a lower field (10^4 V/cm) than that at which breakdown is imminent.)

The second point we would like to make is that the projected Pf^2 is at constant impedance. If lower impedances are realizable within package constraint, higher power will be feasible.

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